What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method for making an ultrathin high-k gate dielectric for use in a field effect transistor comprising:

depositing a high-k gate dielectric material on a substrate; and

forming an ultrathin high-k dielectric by performing a thinning process on said high-k gate dielectric material, wherein the ultrathin high-k dielectric has a thickness of less than about 3 nm.

2. The method of claim 1, wherein the high-k gate dielectric material has a dielectric constant of at least about 7, and the ultrathin high-k gate dielectric has a thickness of less than about 2 nm.

3. The method of claim 2, wherein the high-k gate dielectric material has a dielectric constant ranging from about 10 to about 25, and the ultrathin high-k gate dielectric has a thickness ranging from about 1 nm to about 2 nm.

4. The method of claim 3, wherein the high-k dielectric material is selected from the group consisting of a metal oxide, a metal oxynitride, a metal silicon oxide, a metal silicon oxynitride, a metal germanium oxide, a metal germanium oxynitride, and alloys, mixtures, or multilayers of the same; wherein the metal is selected from the group consisting of Al, Ba, Be, Bi, C, Ca, Ce, Co, Cr, Dy, Eu, Fe, Ga, Gd, Hf, In, La, Li, Mg, Mn, Mo, Nb, Ni, Pr, Sc, Sr, Ta, Ti, V, W, Y, Zn, and Zr.

5. The method of claim 4, wherein the high-k dielectric material comprises HfO_2.

6. The method of claim 4, further comprising depositing at least one interfacial layer of a metal-free dielectric material between the substrate and the high-k gate dielectric.

7. The method of claim 6, wherein the metal-free dielectric material is selected from the group consisting of silicon oxide, germanium oxide, silicon oxynitride, germanium oxynitride, silicon nitride, and germanium nitride.

8. The method of claim 1, wherein the thinning process is selected from the group consisting of wet etching, dry etching, and hybrid damage/wet etching.

9. The method of claim 8, wherein the dry etching process is selected from the group consisting of physical sputtering, ion beam etching, reactive ion etching, and gas cluster ion beam (GCIB) processing.

10. The method of claim 8, wherein the thinning process comprises hybrid damage/wet etching treatment.

11. The method of claim 10, wherein the hybrid damage/wet etching treatment comprises an argon reactive ion etch as the damage treatment.

12. The method of claim 1, further comprising a post-thinning treatment of the high-k dielectric material.

13. The method of claim 12, wherein the post-thinning treatment is selected from the group consisting of annealing in an inert ambient, annealing in a reactive ambient, and treating with plasma.

14. The method of claim 1, further comprising adding additional material to the gate dielectric during or after the thinning, wherein the additional material is selected from the

group consisting of Al, B, Ba, Be, Bi, Br, C, Ca, Ce, Cl, Co, Cr, Dy, Eu, F, Fe, Ga, Gd, Ge, H, Hf, In, La, Li, Mg, Mn, Mo, N, Nb, Ni, O, P, Pr, S, Sc, Si, Sn, Sr, Ta, Ti, V, W, Y, Zn, and Zr.

15. The method of claim 14, wherein the additional material comprises N.

16. The method of claim 1, further comprising annealing said high-k dielectric material prior to performing said thinning process.

17. An ultrathin high-k gate dielectric for use in a field-effect transistor made by a method comprising:

depositing a high-k gate dielectric material on a substrate; and

forming an ultrathin high-k dielectric by performing a thinning process on said high-k gate dielectric material, wherein the ultrathin high-k dielectric has a thickness of less than about 3 nm.

18. The gate dielectric of claim 17, wherein the high-k gate dielectric material has a dielectric constant of at least about 7, and the ultrathin high-k gate dielectric has a thickness of less than about 2 nm.

19. The gate dielectric of claim 18, wherein the high-k gate dielectric material has a dielectric constant ranging from about 10 to about 25, and the ultrathin high-k gate dielectric has a thickness ranging from about 1 nm to about 2 nm.

20. The gate dielectric of claim 19, wherein the high-k dielectric material is selected from the group consisting of a metal oxide, a metal oxynitride, a metal silicon oxide, a metal silicon oxynitride, a metal germanium oxide, a metal germanium oxynitride, and alloys, mixtures, or multilayers of the same; wherein the metal is selected from the group

consisting of Al, Ba, Be, Bi, C, Ca, Ce, Co, Cr, Dy, Eu, Fe, Ga, Gd, Hf, In, La, Li, Mg, Mn, Mo, Nb, Ni, Pr, Sc, Sr, Ta, Ti, V, W, Y, Zn, and Zr.

21. The gate dielectric of claim 20, wherein the high-k dielectric material comprises HfO_2.

22. The gate dielectric of claim 20, wherein the method to make said dielectric further comprises deposition at least one interfacial layer of a metal-free dielectric material between the substrate and the high-k gate dielectric.

23. The gate dielectric of claim 22, wherein the metal-free dielectric material is selected from the group consisting of silicon oxide, silicon oxynitride, and silicon nitride.

24. The gate dielectric of claim 17, wherein the thinning process is selected from the group consisting of wet etching, dry etching, and hybrid damage/wet etching.

25. The gate dielectric of claim 24, wherein the dry etching process is selected from the group consisting of physical sputtering, ion beam etching, reactive ion etching, and gas cluster ion beam (GCIB) processing.

26. The gate dielectric of claim 24, wherein the thinning process comprises hybrid damage/wet etching treatment.

27. The gate dielectric of claim 26, wherein the hybrid damage/wet etching treatment comprises an argon reactive ion etch as the damage treatment.

28. The gate dielectric of claim 17, wherein the method to make said dielectric further comprises a post-thinning treatment of the high-k dielectric material.

29. The gate dielectric of claim 28, wherein the post-thinning treatment is selected from the group consisting of annealing in an inert ambient, annealing in a reactive ambient, and treating with plasma.

30. The gate dielectric of claim 17, further comprising adding additional material to the gate dielectric during or after the thinning, wherein the additional material is selected from the group consisting of Al, B, Ba, Be, Bi, Br, C, Ca, Ce, Cl, Co, Cr, Dy, Eu, F, Fe, Ga, Gd, Ge, H, Hf, In, La, Li, Mg, Mn, Mo, N, Nb, Ni, O, P, Pr, S, Sc, Si, Sn, Sr, Ta, Ti, V, W, Y, Zn, and Zr.

31. The gate dielectric of claim 30, wherein the additional material comprises N.

32. The gate dielectric of claim 17, wherein the method to make said dielectric further comprises annealing said high-k dielectric material prior to performing said thinning process.